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Application No.	10/028,858
Filing Date	December 19, 2001
First Named Inventor	Shivandan Kaushik
Art Unit	2112
Examiner Name	ZAMAN, FAISAL M.
Total Number of Pages in This Submission	
Attorney Docket Number	42390P13163

ENCLOSURES *(check all that apply)*

- ☒ Fee Transmittal Form
  - ☒ Fee Attached
- ☐ Amendment / Response
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
  - ☐ PTO/SB/08
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- ☐ Response to Missing Parts/ Incomplete Application
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  - ☐ Declaration/POA
  - ☐ Response to Missing Parts under 37 CFR 1.52 or 1.53
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SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual name	Paul A. Mendonsa, Reg. No. 42,879 BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
Signature	
Date	August 23, 2006

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Typed or printed name	**Julie Dussault**		
Signature		Date	**August 23, 2006**

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FEE TRANSMITTAL for FY 2005

Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27.

TOTAL AMOUNT OF PAYMENT	($)	500.00

Complete if Known	
Application Number	10/028,858
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METHOD OF PAYMENT *(check all that apply)*

☒ Check ☐ Credit card ☐ Money Order ☐ None ☐ Other (please identify): _____

☒ Deposit Account Deposit Account Number: 02-2666 Deposit Account Name: Blakely, Sokoloff, Taylor & Zafman LLP

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

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FEE CALCULATION

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet.	
2053	130	2053	130	Non-English specification	
1251	120	2251	60	Extension for reply within first month	
1252	450	2252	225	Extension for reply within second month	
1253	1,020	2253	510	Extension for reply within third month	
1254	1,590	2254	795	Extension for reply within fourth month	
1255	2,160	2255	1,080	Extension for reply within fifth month	
1401	500	2401	250	Notice of Appeal	
1402	500	2402	250	Filing a brief in support of an appeal	500.00
1403	1,000	2403	500	Request for oral hearing	
1451		2451		Petition to institute a public use proceeding	
1460	130	2460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
1809	790	1809	395	Filing a submission after final rejection (37 CFR § 1.129(a))	
1810	790	2810	395	For each additional invention to be examined (37 CFR § 1.129(b))	

Other fee (specify) _____

SUBTOTAL (2) ($) 500.00

SUBMITTED BY Complete (if applicable)

Name (Print/Type)	Paul A. Mendonsa	Registration No. (Attorney/Agent)	42,879	Telephone	(503) 439-8778
Signature				Date	08/23/06

Based on PTO/SB/17 (12-04) as modified by Blakely, Sokoloff, Taylor & Zafman (wlr) 12/15/2004.
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of:

Shivnandan D Kaushik et al. for
Intel Corporation

Serial No.:	10/028,858	Group Art Unit:	2112
Filed:	December 19, 2001	Examiner:	ZAMAN, FAISAL M.

FOR: **HOT PLUG INTERFACE CONTROL METHOD AND APPARATUS**

I, Julie Dussault, hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on August 23, 2006.

Julie Dussault
(Signature of person mailing correspondence)

APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicants (hereinafter Appellants) submit this appeal brief, thus perfecting the notice of appeal filed on March 28, 2006. The required headings and subject matter follow.

(i) Real party in interest.

This case is assigned of record to Intel Corporation, who is the real party in interest.

(ii) Related appeals and interferences.

Appellants had filed an appeal brief on July 6, 2005, in response to the Office Action dated February 7, 2005.

(iii) Status of claims.

Claims 1-10, and 16-38 are pending. Claims 16-27 and 31-34 have been allowed and claims 6, 30, 36 and 38 would be allowable if rewritten in independent form to include each and every limitation of the base claim and any intervening claim.

(iv) Status of amendments.

An After Final Response that amended claim 7 was mailed June 26, 2006. The appendix reflects the entry of entered amendment to claim 7.

(v) Summary of claimed subject matter.

Claim 1 relates to a method that comprises identifying one or more caching agents 230, 510 provided by a hot plug module 110 in response to the hot plug module 110 being physically coupled to the running computing device and adding the identified caching agents 230, 510 of the hot plug module 110 to a resource pool of the running computing device (See, blocks 934, 938 of FIG. 9C, paragraphs [0060] and [0062]).

The method further comprises enabling a communication interface 214 of the hot plug module 110 to establish a communication link with a running computer system (See, blocks 1001-1002 of FIG. 9H, paragraphs [0084]-[0085]).

Claim 8 relates to a method that comprises identifying memory 240 of the hot plug module 110 in response to the hot plug module 110 being physically coupled to the running computing device. (See, FIGS. 2, 4, 9C, block 936, paragraph [0061]). The method further comprises adding the identified memory 240 of the hot plug module 110 to a memory pool of the running computing device (See, block 936 of FIG. 9C, paragraph [0061]).

Claim 16 relates to a machine readable medium (paragraph [0048]) for interrupt processing that comprises a plurality of instructions that in response to being executed result in a computing device examining a plurality of interface control registers 706 associated with a plurality of communication interfaces 628 for communicating with a plurality of hot plug modules 110 having caching agents 230, 510 in response to a hot plug interrupt. The machine readable medium further comprises instructions that result in the computing device identifying which of a plurality of hot plug events caused the hot plug interrupt based upon the plurality of interface control registers 706. (See, e.g., FIGS. 7 and 9A, paragraphs [0041], [0049], [0058], [0066] and [0069])

Claim 24 relates to a hot plug module 110 that comprises a coupler 112 for detachably coupling the hot plug module 110 to a running computing device. (FIGS. 1-5). The hot plug module 110 further comprises a communication interface 214 to establish a communication link with the running computing device via the coupler 112 in

response to being enabled and to de-establish the communication link in response to being disabled. (See, block 996 of FIG. 9H, and block 920 of FIG. 9B, paragraphs [0057] and [0081]). The hot plug module 110 also comprises an interface control register 706 associated with the communication interface 214 to indicate and control whether the communication interface 217 is enabled or disabled. (See, paragraph [0042]). The hot plug module 110 further comprises a processor 230 and associated memory cache 232 wherein the processor 230 programs the interface control register 706 to enable and disable the communication interface based upon whether the hot plug module 110 is ready to join the running computing device. (See, FIG. 3 and paragraphs [0042], [0057] and [0081]).

Claim 28 is related to a computing device 100 that comprises a midplane 120, 600 having a coupler 122 and a hot plug interface 626 to track a state associated with the coupler 122. (See, FIGS. 1, 6 and 7, paragraphs [0028], [0038]). The computing device 100 may further comprise a hot plug module 110 comprising a coupler 110 to detachably couple the hot plug module 110 to the coupler 122 of the midplane 120, 600 and resources coupled to the coupler 112 of the hot plug module 110 via a hot plug interface 212 of the hot plug module 110. (See, FIGS. 1-5). The hot plug module 110 updates the state of the hot plug interface 626 of the midplane 120, 600 to indicate when the resources are ready to join the computing device 100. (See, FIG. 1-6 and 9G, paragraph [0079]). The computing device also comprises a processor 230, 636 coupled to the hot plug interface 626 of the midplane 120, 600. The processor 230, 636 adds the resources to the computing device 100 without rebooting in response to determining

that the hot plug interface 626 of the midplane 120, 600 indicates the resources are ready to join (See., FIG. 9C).

Claim 31 relates to a midplane 120 that comprises a plurality of couplers 122 to detachably couple hot plug modules 110 to the midplane 120 and at least one switch 624 to interconnect the plurality of couplers 122. (See, FIG. 6). The switch 624 comprises a plurality of communication interfaces 628 to establish communication links with the hot plug modules 110 that are coupled to the plurality of couplers 122, and a plurality of interface control registers 706 to control the plurality of communication interfaces 628 (See, Figs. 1, 6 and 7, paragraphs [0028]-[0031] and [0041]).

Claim 35 relates to the method of claim 3, further comprising transferring packets between the communication interface on the hot plug module and the communication interface of the running computer system to establish the communication link (See paragraphs [0062] - [0064] and [0076], [0077].

(vi) Grounds of rejection to be reviewed on appeal

Whether claims 1, 7-9 under 35 USC 102(e) are anticipated by Olarig et al. (US Patent 6,587,909).

Whether claims 1-5, 7-10, 28-29, 35 and 37 under 35 USC 102(e) are anticipated by Bealkowski et al. (US Patent 6,282,596).

(vii) Argument.

Claim Rejection under 35 USC 102 (Olarig)

The Official Action rejected claims 1, 7-9 under 35 USC 102(e) as being anticipated by Olarig et al. (US Patent 6,587,909). Appellants respectfully request allowance of claims 1 and 7-9.

As is well-established, in order to successfully assert a *prima facie* case of anticipation, the Official Action must provide a single prior art document that includes every element and limitation of the claim or claims being rejected. Therefore, if even one element or limitation is missing from the cited document, the Official Action has not succeeded in making a prima facie case.

Claims 1 and 7-9

Each of claims 1 and 7-9 require enabling a communication interface ***on a hot plug module*** to establish a communication link with a running computing device. Olarig in the cited column 5, lines -27 discloses that advanced configuration power interface (ACPI) responds to system control interrupt (SCI) by calling the control method associated with a "hot add" memory event. The "hot add" memory control method may determine if memory has been added or removed, read the memory configuration to determine the type and amount of memory, check whether the newly added memory is compatible with the current memory configuration and configure and initialize the last added DIMM and set status bit to indicate to the memory controller that new memory has been added and notify the OS via ACPI driver of the hot addition of memory.

Olarig, thus teaches a hot add memory control method wherein the ACPI driver responds to the SCI by calling the control method associated with a hot add memory event. Olarig, however, does not appear to teach enabling a communication interface ***on the hot plug module*** as required by claims 1 and 7-9.

The Examiner appears to equate Olarig's disclosure, "circuitry on the memory module is fully turned on before the circuitry is driven by a clock signal" in column 6, lines 50-57 with "enabling a communication interface ***on a hot plug module*** to establish a communication link with a running computing device".

However, in contrast with the claimed invention, Olarig merely discloses a power up sequence for slot connector that holds an SDRAM memory module. The memory controller first provides power to the slot connector by connecting the power lines to the slot connector. The memory controller then connects the clock line to the slot connector. As the clock line is connected to the slot connector after power lines, circuitry on the memory module is fully turned on before the circuitry is driven by a clock signal. Olarig thus teaches the process to turn on the circuitry on the memory module before the circuitry is driven by a clock signal.

Appellants submit that a person skilled in the art would not interpret "circuitry on the memory module is fully turned on before the circuitry is driven by a clock signal" as being similar to "enabling a communication interface ***on a hot plug module*** to establish a communication link with a running computing device. "Since Olarig does not teach enabling a communication interface ***on the hot plug module*** to establish a

communication link with a running computing device, Olarig does not anticipate claims 1 and 7-9. Appellants respectfully request the rejection of claims 1 and 7-9 be reversed.

Claim Rejection under 35 USC 102 (Bealkowski)

The Official Action rejected claims 1-5, 7-10, 28-29, 35 and 37 under 35 USC 102(e) as being anticipated by Bealkowski et al. (US Patent 6,282,596). Appellants respectfully request allowance of claims 1-5, 7-10, 28-29, 35 and 37.

As is well-established, in order to successfully assert a *prima facie* case of anticipation, the Official Action must provide a single prior art document that includes every element and limitation of the claim or claims being rejected. Therefore, if even one element or limitation is missing from the cited document, the Official Action has not succeeded in making a prima facie case.

Claims 1, 5 and 8

Each of the claims 1, 5 and 8, require enabling a communication interface ***on the hot plug module*** to establish a communication link with a running computing device. In column 3, lines 1-15, Bealkowski discloses that in the bus architectures, it would be preferable that the processor cards and/or voltage regulator module are hot-pluggable in order that the processor configuration may be reconfigured while power is applied to a personal computer or server. It is important when making changes to a system bus that the bus impedance is maintained (Fig. 1). Further, in column 3, lines 35-41 Bealkowski discloses that initialization routine are performed on the processor with in the processor subsystem through a controller which transmits initialization data to the

processor independent of the system bus, such that additional processor subsystems are integrated into the data processing system with minimal effect on any existing processors operating on the system bus.

Bealkowski appears to teach a hot-pluggable system bus 18 for processor cards 11a-11d. However, the processor cards 11a-11d appear not to have a communication interface. Thus, Bealkowski appears to provide no teaching regarding enabling a communication interface of the processor cards 11a-11d which are **presumably being equated** by the Examiner with the "hot plug module" limitation of claims 1 and 8.

Bealkowski discloses FET switches 82, 86 to control power supplied to the processor cards 11a-11d. Bealkowski further discloses a clock buffer to control application of clock signals to the processor cards 11a-11d. Moreover, Bealkowski discloses FET switches 80 that provide front-side isolation to maintain electrical integrity during hot-plug. However, as clearly depicted in Bealkowski's FIGS. 3A and 3B, the FET switches 80, 82, 86 and the clock buffer are all on the computer system side of the CPU connectors 14 and are not part of the processor cards 11a-11d.

The Examiner in the office action states, "a communication interface ***on the hot plug module*** is inherent, since the hot plug module is coupled to CPU connectors 14". Further, Examiner has relied upon the Appellants' arguments in page 14 lines 19-22 of the last response. Appellants believe the Examiner is relying on the CPU connectors 14 and the inherent idea that the processor cards 11 must have an interface for mating with the CPU connectors 14. However, even if the processor cards 11 inherently have an interface for mating with the CPU connectors 14, Bealkowski does not ***explicitly or***

inherently teach that such an ***interface is enabled*** in order to establish a communication link".

Bealkowski explicitly teaches using FET switches 80, 82, 86 to control the signaling between the processor cards 11a-11d and the computer system. Such FET switches 80, 82, 86 are sufficient to provide the isolation described by Bealkowski. As a result, there is no reason to believe that the interfaces of the processor cards 11 have the capability of being enabled.

Since Bealkowski does not teach enabling a communication interface ***on a hot plug module*** as required by Appellants' claims 1, 5 and 8. Appellants respectfully request the rejection of claims 1, 5 and 8 be reversed.

Claims 2-4

Each of claims 2-4 depends from claim 1. Accordingly, each of claims 2-4 is allowable for at least the reasons stated above in regard to claim 1. Furthermore, each of claims 2-4 requires **both** a communication interface ***on the hot plug module*** and a communication interface ***of a running computer system*** to establish the communication.

In the office action, the Examiner states that Bealkowski discloses enabling communication interface based Fig. 3 item 14a-d. Appellants submit that item 14a-d is the CPU connector and is used to interface processor cards 11a-11d with the CPU connector 14a-d. Further, Bealkowski in the cited column 3, lines 27-29, discloses a method and system for hot plugging a processor sub-system to system bus of a data processing system. The examiner appears to equate CPU connector 14 of Bealkowski

with communication interface of a hot plug module of the Appellants. Appellants submit that a person skilled in the art would not treat a CPU connector 14 as being similar to the communication interface of the hot plug module.

Further, Bealowaski in Fig. 4 and the related description discloses a process for controlling the addition of a hot plug processor subsystem including a processor card and associated voltage regulator module (VRM). Appellants have been unable to locate where Bealkowski teaches both a communication interface ***on the hot plug module*** and a communication interface ***of a running computer system*** to establish the communication.

Since Bealkowski does not teach each and every limitation of the Appellants' claims 2-4, Bealkowski does not anticipate claims 2-4. Appellants respectfully request the rejection of claims 2-4 be reversed.

Claim 7

Claim 7 depends from claim 1. Accordingly, claim 7 is allowable for at least the reasons stated above in regard to claim 1. Furthermore, claim 7 requires adding the identified memory of the hot plug module to a ***memory pool to increase the memory pool***. Appellants are unable to locate where Bealkowski teaches adding the identified memory of the hot plug module to a memory pool ***to increase capacity of the memory pool***.

In the office action, the Examiner states that Bealkowski, in column 9, lines 42-45, teaches adding memory from a hot plug module to a memory pool. Appellants submit that Bealkowski, in column 9, lines 42-45, only teaches that in removing the

processor from operation, the work load is quiesced from the processor, the caches of the processor are flushed and the processor is set to idle. Bealkowski does not appear to teach, "identifying memory of the hot plug..... memory is allocated to process", as mentioned by the examiner in the office action. Further, Appellants submit that the reasons stated above in regard to claim 1 are applicable to the patentability of claim 7. Appellants respectfully request the rejection of claim 7 be reversed.

Claims 28

Claim 28 requires a midplane having a hot plug interface and a hot plug module to update the state of the hot plug interface of the midplane to indicate when the resources are ready to join the computing device. Appellants submit that in column 1, lines 57-58, Bealkowski discloses that with the advent of "hot plug" adaptor, the configuration of computer system may be alerted with rebooting. Bealkowski, does not appear to teach, "the processor to add the resource to the computing device..... resources are ready to join", as suggested by the examiner in the official action.

Further, in column 5, lines 41-52, Bealkowski discloses the control functions of the hot plug controller 70 and LED service indicators. Again, Bealkowski does not appear to teach, "hot plug module to update the state of the hot plug interface of the midplane to indicate when the resources are ready to join the computing device" as suggested by the examiner in the office action. Appellants have been unable to locate where Bealkowski teaches a hot plug module that updates a hot plug interface of a midplane as required by claim 28.

In the office action, the Examiner states that since Bealkowski teaches enabling a communication interface on the hot plug module, it teaches the limitation of claim 28 of the Appellants. Appellants respectfully submit that Bealkowski does not appear to teach enabling a communication interface on the hot plug module and a hot plug module to update the state of the hot plug interface of the midplane to indicate when the resources are ready to join the computing device.

Appellants further submit that Bealkowski merely indicates that a service processor and/or a hot plug control of the computer system side of the connector manage FET switches that isolate a processor card during addition and removal. There appears to be no teaching of the processor card updating a hot plug interface on the computer system side of the connector. Since Bealkowski does not teach each and every limitation of claim 28, Bealkowski does not anticipate Appellants' claim 28. Appellants respectfully request the rejection of claim 28 be reversed.

Claims 29

Claim 29 depends from claim 28. Accordingly, claims 29 is allowable for at least the reasons stated above in regard to claim 28. Furthermore claim 29 requires hot plug interface of the midplane to generate a hot plug interrupt in response to a change in the signal that is indicative of whether the coupler of the hot plug module has been coupled to the coupler of the midplane. Appellants have reviewed Bealkowski in detail and are unable to locate the limitation.

Since Bealkowski does not teach each and every limitation of claim 29, Bealkowski does not anticipate Appellants' claim 29. Appellants respectfully request the rejection of claim 29 be reversed.

Claim 35

Claim 35 depends from claim 1. Accordingly, claim 35 is allowable for at least the reasons stated above in regard to claim 1. Furthermore, claim 35 requires transferring packets between the communication interface on the hot plug module and the communication interface of the running computer system. Appellants have reviewed Bealkowski in detail and are unable to locate the limitation of claim 35. Since Bealkowski does not teach each and every limitation of claim 35, Bealkowski does not anticipate Appellants' claim 35. Appellants respectfully request the rejection of claim 35 be reversed.

Claim 37

Claim 37 depends from claim 8. Accordingly, claim 37 is allowable for at least the reasons stated above in regard to claim 8. Furthermore, claim 37 requires transferring packets between the communication interface on the hot plug module and the communication interface of the running computer system. Appellants have reviewed Bealkowski in detail and are unable to locate the limitation of claim 37. Since Bealkowski does not teach each and every limitation of claim 37, Bealkowski does not anticipate Appellants' claim 37. Appellants respectfully request the rejection of claim 37 be reversed.

CONCLUSION

In view of the foregoing, favorable reconsideration and reversal of the rejections is respectfully requested. Early notification of the same is earnestly solicited. If there are any questions regarding the present application, the Examiner and / or the Board is invited to contact the undersigned attorney at the telephone number listed below.

Respectfully submitted,

August 23, 2006
Date

Paul A. Mendonsa
Reg. No. 42,879

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(viii) Claims appendix.

What is claimed is:

1. (Previously Presented) A method of adding one or more caching agents to a running computing device, comprising

identifying the one or more caching agents provided by a hot plug module in response to the hot plug module being physically coupled to the running computing device;

adding the identified caching agents of the hot plug module to a resource pool of the running computing device; and

enabling a communication interface on the hot plug module to establish a communication link with the running computing device.

2. (Original) The method of claim 1, further comprising

enabling a communication interface of the running computing device that is associated with the hot plug module in response to determining that the hot plug module has been physically coupled to the running computing device.

3. (Previously Presented) The method of claim 2, further comprising

performing a self test of the hot plug module, and

in response to passing the self test, enabling the communication interface of the hot plug module to establish the communication link with the communication interface of the running computing device.

4. (Original) The method of claim 2, further comprising

initializing the hot plug module, and

after initializing the hot plug module, enabling the communication interface of the hot plug module to establish the communication link with the communication interface of the running computing device.

5. (Original) The method of claim 1 wherein adding comprises adding one or more memory caching processors of the identified caching agents to a processor pool of the running system.

6. (Original) The method of claim 1 wherein adding comprises adding one or more memory caching input/output hubs of the identified caching agents to an input/output pool of the running system.

7. (Currently Amended) The method of claim 1 further comprising

identifying memory of a hot plug module in response to the hot plug module being physically coupled to the running computing device; ~~and~~ and

adding the identified memory of the hot plug module to a memory pool of the running computing device to increase the memory pool from which memory is allocated to processes.

8. (Previously Presented) A method of adding memory to a running computing device, comprising

identifying memory of a hot plug module in response to the hot plug module being physically coupled to the running computing device;

adding the identified memory of the hot plug module to a memory pool of the running computing device to increase the memory pool from which memory is allocated to threads, and

enabling a communication interface on the hot plug module to establish a communication link with the running computing device.

9. (Original) The method of claim 8, further comprising

enabling a communication interface of the running computing device that is associated with the hot plug module in response to determining that the hot plug module has been physically coupled to the running computing device.

10. (Previously Presented) The method of claim 8, further comprising

performing a self test of the hot plug module, and

in response to passing the self test, enabling a communication interface of the hot plug module to establish a communication link with the communication interface of the running computing device.

11-15. (Canceled)

16. (Original) A machine readable medium for interrupt processing, comprising a plurality of instructions that in response to being executed result in a computing device

in response to a hot plug interrupt examining a plurality of interface control registers associated with a plurality of communication interfaces for communicating with a plurality of hot plug modules having caching agents; and

identifying which of a plurality of hot plug events caused the hot plug interrupt based upon the plurality of interface control registers.

17. (Original) The machine readable medium of 16, wherein the plurality of instructions in response to being executed further result in the computing device

determining whether hot plug addition or hot plug removal has been requested for a hot plug module of the plurality of hot plug modules based upon an interface control register of the plurality of interface control registers that is associated with the hot plug module.

18. (Original) The machine readable medium of claim 17, wherein the plurality of instructions in response to being executed further result in the computing device

determining that hot plug removal has been requested for the hot plug module in response to the interface control register associated with the hot plug module indicating a pending hot plug interrupt and a joined state for the hot plug module.

19. (Original) The machine readable medium of claim 18, wherein the plurality of instructions in response to being executed further result in the computing device

causing the hot plug module to write back modified cache lines to the running computing device; and

removing resources of the hot plug module from the computing device.

20. (Original) The machine readable medium of claim 16, wherein the plurality of instructions in response to being executed further result in the computing device

determining that hot plug removal has been requested for the hot plug module;

waiting a predetermined time for pending transactions associated with hot plug module to complete; and

disabling the communication interface of the computing device to isolate the hot plug module from the computing device after waiting the predetermined time.

21. (Original) The machine readable medium of claim 16, wherein the plurality of instructions in response to being executed further result in the computing device

determining that hot plug removal has been requested for the hot plug module; and

disabling the communication interface of the computing device to isolated the hot plug module from the computing device after determining that all transactions associated with the hot plug module have completed.

22. (Original) The machine readable medium of claim 16, wherein the plurality of instructions in response to being executed further result in the computing device

determining that hot plug addition has been requested for the hot plug module in response to the interface control register indicating that the associated communication interface is disabled, that a module is coupled to the associated communication interface, and that the associated communication interface is in a no module present state.

23. (Original) The machine readable medium of claim 22, wherein the plurality of instructions in response to being executed further result in the processor

adding resources of the hot plug module to the running computing device in response to determining that hot plug addition has been requested for the hot plug module and that no other hot plug addition is in progress.

24. (Original) A hot plug module comprising

a coupler for detachably coupling the hot plug module to a running computing device;

a communication interface to establish a communication link with the running computing device via the coupler in response to being enabled and to de-establish the communication link in response to being disabled;

an interface control register associated with the communication interface to indicate and control whether the communication interface is enabled or disabled, and

a processor and associated memory cache, the processor to program the interface control register to enable and disable the communication interface based upon whether the hot plug module is ready to join the running computing device.

25. (Original) The hot plug module of claim 24, wherein

the processor writes back modified cache lines of the memory cache to the running computing device in response to hot plug removal being requested for the hot plug module.

26. (Original) The hot plug module of claim 25, wherein the hot plug module comprises a status indicator that indicates a hot plug status for the hot plug module.

27. (Original) The hot plug module of claim 26, wherein the processor

performs a self test of the hot plug module in response to hot plug addition being requested for the hot plug module, and

enables the communication interface in response to determining that the hot plug module passed the self test.

28. (Original) A computing device comprising,

a midplane comprising a coupler and a hot plug interface to track a state associated with the coupler;

a hot plug module comprising a coupler to detachably couple the hot plug module to the coupler of the midplane and resources coupled to the coupler of the hot plug module via a hot plug interface of the hot plug module, the hot plug module to update the state of the hot plug interface of the midplane to indicate when the resources are ready to join the computing device, and

a processor coupled to the hot plug interface of the midplane, the processor to add the resources to the computing device without rebooting in response to determining that the hot plug interface of the midplane indicates the resources are ready to join.

29. (Original) The computing device of claim 28, wherein

the midplane comprises a hot plug monitor that provides the hot plug interface of the midplane with a signal indicative of whether the coupler of the hot plug module has been coupled to the coupler of the midplane, and

the processor programs the hot plug interface of the midplane to generate a hot plug interrupt in response to a change in the signal that is indicative of whether the coupler of the hot plug module has been coupled to the coupler of the midplane.

30. (Original) The computing device of claim 28, wherein

the hot plug interface of the midplane detects whether framing packets are received from the hot plug interface of the hot plug module, and

the processor programs the hot plug interface of the midplane to generate a hot plug interrupt in response to a change in receipt of framing packets.

31. (Original) A midplane of a computing device, comprising

a plurality of couplers to detachably couple hot plug modules to the midplane;

at least one switch to interconnect the plurality of couplers, the at least one switch comprising a plurality of communication interfaces to establish communication links with the hot plug modules that are coupled to the plurality of couplers, and a plurality of interface control registers to control the plurality of communication interfaces.

32. (Original) The midplane of claim 31, further comprising a system management processor to initialize hot plug modules coupled the plurality of couplers.

33. (Original) The midplane of claim 32, wherein the plurality of interface control registers track states of the plurality of communication interfaces and associated hot plug modules.

34. (Original) The midplane of claim 31, wherein the switch provides an indication as to when all pending transactions associated with a hot plug module to be removed have completed.

35. (Previously Presented) The method of claim 3, further comprising transferring packets between the communication interface on the hot plug module and the communication interface of the running computer system to establish the communication link.

36. (Previously Presented) The method of claim 3, further comprising determining that the communication link has been established in response to transferring a predetermined number of error free packets between the communication interface on the hot plug module and the communication interface of the running computer system.

37. (Previously Presented) The method of claim 9, further comprising transferring packets between the communication interface on the hot plug module and the communication interface of the running computer system to establish the communication link.

38. (Previously Presented) The method of claim 9, further comprising determining that the communication link has been established in response to transferring a predetermined number of error free packets between the communication interface on the hot plug module and the communication interface of the running computer system.

(ix) Evidence appendix.

None.

(x) Related proceedings appendix.

None.